COMSATS University Islamabad, Vehari Campus
Department of Computer Science
Sessional-II Spring-19

Class: BSCS/BSSE
Subject: Digital Logic Design
Total Time Allowed: 1.5 hour
Name: Ahmer Iqbal

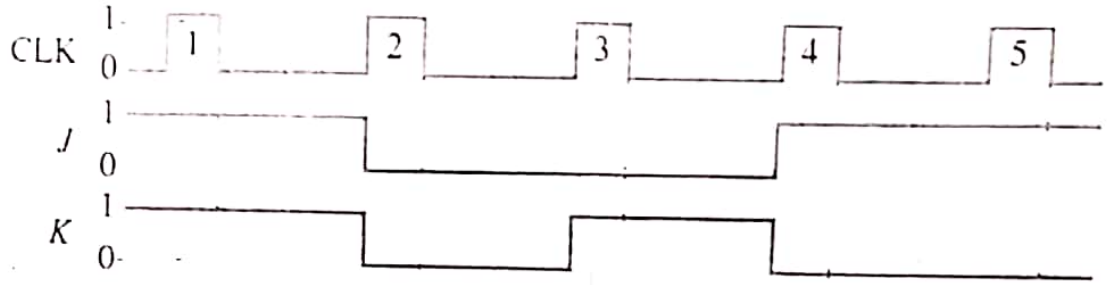
Date: 02-05-2019
Instructor: M Rehan Ashraf
Max Marks: 30
Registration# SP18-BSE-002

Note: Attempt all questions, be specific and to the point. Clearly show the detail of your work.

Q#01: Design a controlled adder/subtractor which can add/subtract two nibbles. Clearly show the detail of your work. (8)

Q#02: a) Draw the circuit diagram of a positive edge triggered JK flip flop. Clearly show the timing diagram of all the possible states. (7)

b) The waveform in figure given below is applied to the negative edge triggered JK flip flop. Draw the timing diagram of output Q. Assuming that the flip flop is initially reset. (7)



Q#03: a) Draw the circuit diagram of a D flip flop. Discuss all the possible combinations of inputs along with clock. (4)

b) Draw the output Q for the input given in the figure below. (4)