COMSATS University Islamabad, Vehari Campus
Department of Computer Science
Final Paper Spring-19

Class: BSCS/BSSE
Subject: Digital Logic Design
Total Time Allowed: 3 Hours.
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Date: 17-06-2019
Instructor: M Rehan Ashraf
Max Marks: 50
Registration# SP18-BSE-002

Note: Attempt all questions, be specific and to the point. Clearly show the detail of your work.

Q#01: Short Questions

a) Design a combinational logic circuit that has four inputs and one output. The output is equal to 1, when input is greater than 1000. (2)

b) Implement $Y=AB+CD$ using NAND gates only. (2)

c) Differentiate the following (2)
1) Latch Vs Flip Flop, 2) Sequential Circuits Vs Combinational Circuits
3) Analog Devices Vs Digital Devices, 4) Volatile Vs Nonvolatile memory

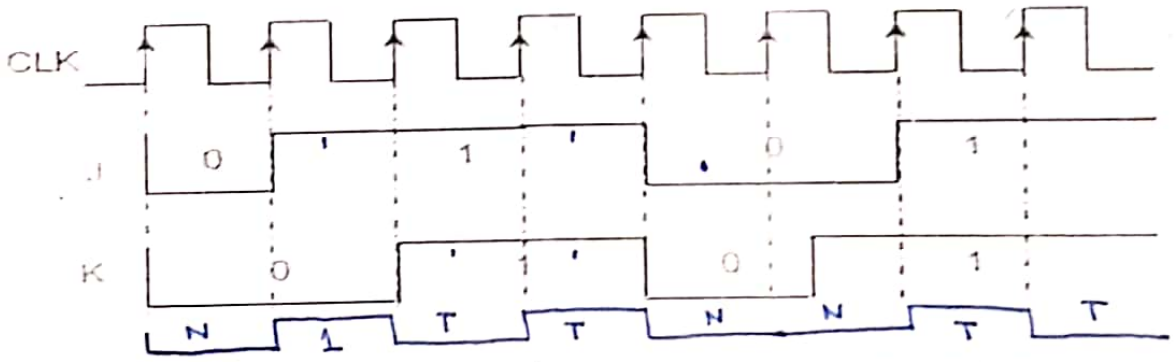
d) Why the gates are called decision making elements? How many input signals can a gate have? How many output signals? (2)

e) What is the main difference between inverter and controlled inverter? Show the circuit diagram of a controlled inverter. (2)

f) Define the following (2)
Chunking, Propagation Delay Time, Setup Time, Hold Time

Q#02: a) Draw the circuit diagram of a negative edge triggered JK flip flop. (2)

b) Draw the output of the positive edge triggered flip flop for the inputs given below. Clearly show the timing diagram of output for all the possible states. (6)



Q#03: a) Design a synchronous/asynchronous down counter which counts from 15 to 0. Clearly show the timing diagram of all the states. (7)

b) Modify the designed counter in part a so that it starts from 7 and down counts up to 0. (5)

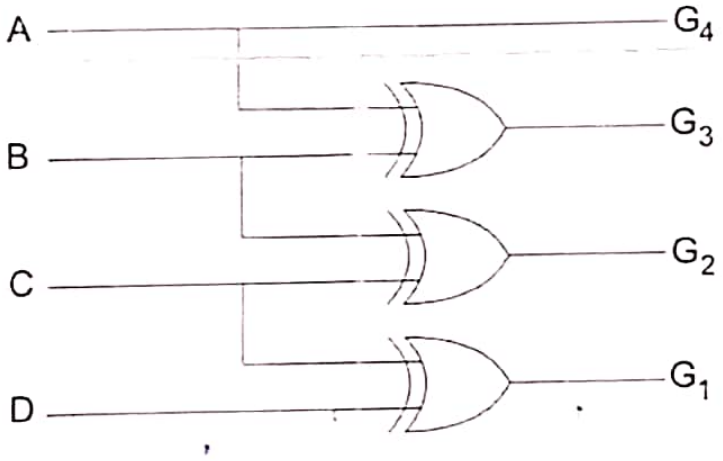
Q#04: Use the Karnaugh Map method to implement the minimum SOP expression for the logic function specified in the truth table given below. (8)

$Y = \bar{A}C + \bar{A}D + BD + A\bar{B}\bar{D}$

	A	B	C	D	F	
0	0	0	0	0	0	m_0
1	0	0	0	1	1	m_1
2	0	0	1	0	1	m_2
3	0	0	1	1	1	m_3
4	0	1	0	0	0	m_4
5	0	1	0	1	1	m_5
6	0	1	1	0	1	m_6
7	0	1	1	1	1	m_7
8	1	0	0	0	1	m_8
9	1	0	0	1	0	m_9
10	1	0	1	0	1	m_{10}
11	1	0	1	1	0	m_{11}
12	1	1	0	0	0	m_{12}
13	1	1	0	1	1	m_{13}
14	1	1	1	0	0	m_{14}
15	1	1	1	1	1	m_{15}

Q#05: a): Draw the circuit diagram of a hexadecimal encoder. (5)

b): Calculate the output of the circuit given below for all input combinations. (5)



GOOD LUCK